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		First Named Inventor	Ming-Dou Ker
		Art Unit	2815
		Examiner Name	J. A. Fenty
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ENCLOSURES (Check all that apply)

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Date	January 4, 2006	Reg. No.	32,334



PATENT
0941-0316P

IN RE APPLICATION OF

BEFORE THE BOARD OF APPEALS

Ming-Dou KER et al.

Appeal No.:

APPL. NO.: 09/944,171

GROUP: 2815

FILED: September 4, 2001

EXAMINER: Jesse A. Fenty

CONF.: 9842

FOR: ESD PROTECTION CIRCUIT WITH VERY LOW INPUT
CAPACITANCE FOR HIGH-FREQUENCY I/O PORTS

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 4, 2006

Sir:

In response to the Notice of December 19, 2005, Appellants are resubmitting the Appeal Brief with two additional Appendices. Each of these appendices have no content as indicated by the word "None." Appellants have added these Appendices as required by the Notice, even though Appellants submit that the requirement is improper.

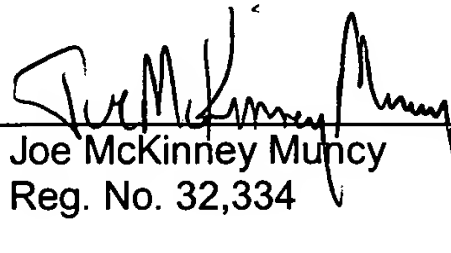
It should be remembered that the Appeal Brief at issue was filed on March 1, 2004, some 5 months before the introduction of the new rules for Appeal Briefs which came into effect in August of 2004. Appellants submit that the Appeal Brief as filed met the requirements for Appeal Briefs which were in force at the time of the filing of the Appeal Brief. Accordingly, Appellants submit that the requirement in the Notification is improper and not necessary. Nevertheless, Appellants have added the two Appendices in order to further the prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
BIRCH STEWART KOLASCH & BIRCH LLP

Date: January 4, 2006

By

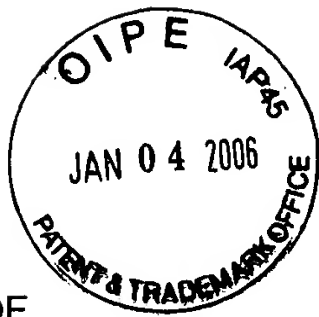

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APPEAL BRIEF
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FOR: ESD PROTECTION CIRCUIT WITH VERY LOW INPUT
CAPACITANCE FOR HIGH-FREQUENCY I/O PORTS

APPEAL BRIEF ON BEHALF
OF APPELLANTS:
MING-DOU KER ET AL.

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

January 4, 2006

Sir:

This is the Appellants' brief in response to a Final Rejection mailed July 29, 2003 finally rejecting claims 1-17. A copy of the claims appealed are attached as an Appendix. The fee of \$330.00 for filing a brief in support of an appeal under 37 C.F. R. § 1.17(f) is submitted herewith.

I. REAL PARTY IN INTEREST

The present application is assigned to Taiwan Semiconductor Manufacturing Co., Ltd. as recorded on September 4, 2001 at Reel 102142, Frames 0370 and 0371. No further assignments of this application have been made.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences for this application.

III. STATUS OF CLAIMS

Claims 1-26 are pending in this application. Claims 18-26 have been withdrawn from consideration is being drawn to a non-elected species. The Election of Species Requirement was presented in the action of October 21, 2002. Remaining claims 1-17 are still under consideration and are being appealed.

IV. STATUS OF AMENDMENTS

Applicants submitted responses After Final Rejection on October 1, 2003 and December 1, 2003, both of which included only remarks. According to the Advisory Actions of October 22, 2003 and January 8, 2004, the Requests for Reconsideration have been considered but do not place the application into condition for allowance.

V. SUMMARY OF THE INVENTION

The present invention relates to an electrostatic discharge (ESD) protection circuit for an integrated circuit device. Integrated circuits are easily damaged by an electrostatic discharge and accordingly, protection devices have been implemented in order to prevent damage to the device. Figs. 1A and 1B show two different types of prior art devices. In these systems, a diode is placed between the input/output pad 10 and each of the voltage lines VDD and VSS. Another set of diodes 16 may be placed between the internal circuit and the same voltage lines. Fig. 5 shows the equivalent circuit of Fig. 1A with the parasitic capacitance also being shown.

The present invention is an improvement on these prior art devices in an attempt to provide the same level of ESD protection but with a small parasitic capacitance. Fig. 6 shows a first embodiment of the present invention and specifically includes a pair of stacked

diodes between the pad and the voltage lines in each direction. Thus, the single diode has been replaced by a pair of diodes placed head to tail. This causes the parasitic capacitance to be lowered. A clamp circuit 34 is also included.

Fig. 13 shows a second embodiment to which the present claims are directed. This embodiment also shows the stacked diodes but also provides a plurality of diodes $D_{R1} \dots D_{R4}$ stacked between the M_{ESD} gate and voltage line VSSA. When the static discharge occurs, inverter 38 provides current to the base of the parasitic bipolar junction transistor and at the same time pulls up the M_{ESD} gate to the clamp voltage limited by the diodes stacked between the gate and VSSA. This increases the turn-on rate of the clamp circuit 34 by applying a bias voltage to the gate of the M_{ESD} . Thus, inverter 38 not only provides a bias current into the substrate of the M_{ESD} , but also provides the bias voltage to the gate. By reducing the equivalent capacitance, the frequency response of the input 4 can be effectively improved.

The clamp circuit 34 includes a delay circuit 36, an inverter 38 and a bipolar junction transistor. The clamp detects the occurrence of the static discharge to turn on the bipolar junction transistor and prevent damage.

In order to achieve this configuration, a specific arrangement of semiconductor layers is provided, as shown in Figs. 11 and 12 in regard to the embodiment of Fig. 6 and in Figs. 16 and 17 with regard to the embodiment of Fig. 13. Thus, in Fig. 16, a deep N well 70 is formed on a P substrate, on which a P-well 66 is formed linked on either side by an N well 68. An N+ doped region is formed in each N well 68 to form a contact for voltage VDDA. The P well includes two N+ regions for the source and drain electrodes and a P+ region for the bulk of the transistor.

VI. ISSUES

(1) Whether the Examiner was correct in rejecting claims 1, 13, 14, 16 and 17 as being anticipated by Jun et al. (U.S. Patent 6,406,948), and especially whether Fig. 10 of Jun et al. shows stacked diodes.

(2) Whether the Examiner was correct in rejecting claims 2-4 as being obvious over Jun et al.

(3) Whether the Examiner was correct in rejecting claims 5-12 and 15 as being obvious over Jun et al. in view of Watt (U.S. Patent 5,623,156).

VII. GROUPING OF CLAIMS

1. Claim 1, the only independent claim.
2. Claims 13-17.
3. Claims 2 and 4.
4. Claim 3.
5. Claims 5, 11 and 12.
6. Claims 6, 7 and 8.
7. Claims 9 and 10.

VIII. ARGUMENTS

Rejection of claim 1 as being anticipated by Jun et al.

The Examiner states that Jun et al. shows an ESD protection circuit with low input capacitance between a power line and an I/O pad, comprising a plurality of diodes stacked and coupled between a first power line and the I/O pad wherein during normal operation, the diodes are reversed biased, and when an ESD event occurs between a second power

line and the I/O pad, the diodes are forward biased to conduct ESD current. In regard to the plurality of diodes, the Examiner particularly refers to Fig. 10 as showing stacked diodes.

Applicants question whether the Jun et al. reference indeed means to show stacked diodes in Fig. 10. Fig. 10 is very briefly described in column 2, lines 32 and 33 as a schematic representation of an electrostatic discharge protection network of the present invention. It is also described on column 3, lines 57-59 as a schematic of the ESD protection network of the present invention. It also states there that the numbered areas relate the schematic to the cross section in Fig. 9 and that the 50 is a polysilicon line. There is no other description of Fig. 10 within the patent.

Admittedly, Fig. 10 of the patent itself could be a basis for this rejection, if indeed this figure does not contradict the remaining parts of the specification. However, Applicants submit that, in fact, the description of the remaining figures is contradictory to the possibility of having stacked diodes in Fig. 10 and that instead the Patentee has used this symbol to indicate a large area of diodes instead.

It is noted that column 3, lines 47 and 48 and line 53 refer to these as large area diodes in regard to Fig. 9. Applicants suggest that the Patentee has used an incorrect symbol to indicate large area diodes and that Fig. 10 only appears to describe stacked diodes. Applicants submit that this is the case based on the description below of the remaining parts of the specification and how this cannot lead to stacked diodes. Applicants point out MPEP 716.07 which indicates that when there is an error that would have been obvious to one of ordinary skill in the art, that the erroneous material is not put in the possession of the public. Applicants submit that this is the case in the present situation.

In regard to Fig. 10, it is noted that ovals are indicated at four points with the reference numerals indicating areas 10, 12, 14 and 16. These refer to the various reference numerals in Fig. 9. Therefore, one set of diodes is formed between substrate 10 and N+ region 14. Since these two regions are adjacent in Fig. 9 and of opposite conductivity type, it would appear that a single diode would be involved. Likewise, N well 12 and P+ region 16 are likewise adjacent and have opposite conductivity so that a single diode would also be appropriate between the ovals in Fig. 10. Thus, it would appear that stacked diodes would not be appropriate.

Applicants have also submitted a copy of Fig. 9 with markings added to help describe a correct understanding of this device. In this explanatory figure, the source/drain regions 32 and the wells which are formed thereunder are marked. The source/drain regions on the left side are indicated as 32L and those on the right side as 32R. The well under regions 32L indicated by 39L, while the well under 32R is indicated as 39R. As indicated in the specification, layer 18 is silicon oxide, as is layer 24. The silicon substrate 10 is P-type. If well 39R is P-type silicon, it will provide a dc short path between P+ region 16 and P substrate 10. In Fig. 10, P+ region 16 and P substrate 10 must be separated by diodes. Therefore, well 39R must be N-type silicon and source/drain 32R must be P-type silicon to form a PMOS.

Further, the attached marked-up Fig. 9 indicates the possible diodes which have been added with diode D1 formed between N+ region 14 and P substrate 10, diode D2 between N+ region 14 and P well 39L, diode D3 between P well 39L and the N source/drain region 32L, diode D4 between P substrate 10 and N well 12, diode D5 between P region 16 and N well 12 and diode D6 between P source/drain region 32R and N well 39.

The equivalent diodes between N region 14 and P substrate 10 are diodes D1, D2, and D3 but all of these diodes are connected in parallel and not in series as shown in Fig. 10. The equivalent diodes between P region 16 and N well 12 are diodes D4, D5 and D6, and these diodes are connected in parallel and not in series as shown in Fig. 10. Thus, given this information, it is clear that there are no stacked diodes in Fig. 9, contrary to the drawing of Fig. 10. Accordingly, one skilled in the art would know that the drawing symbols used in Fig. 10 is actually incorrect and that each diode stack should be replaced with a single diode according to the description in the specification of Fig. 9.

In the Advisory Action, the Examiner explains that the Fig. 10 circuit only appears to represent the relationship of the regions within the lower substrate and concludes that the two equivalent circuits are uncorrelated. If the Examiner were right in this point, there must be at least two diodes connected in a series between two nodes and having the same polarity within the lower substrate 10 of Fig. 9 and the two nodes in Fig. 9 should be the same nodes in Fig. 10.

It is very easy to perceive the error since there are only three diodes in the lower substrate 10 marked as D1, D4 and D5. In order for the diodes to be stacked as shown in Fig. 10, only D1 and D5 can fit and D4 must be excluded since it is connected in reverse polarity. D1 and D5 are connected in series between P+ region 16 and N+ region 14 in Fig. 9. The series connection of D1 and D5 between nodes 16 and 14 is inconsistent with what is depicted in Fig. 10 where no diode exists between node 16 and node 14.

Obviously, one skilled in the art can understand that the stacked diodes cannot be achieved from the arrangement shown in Fig. 9. Accordingly, Applicants submit that the Examiner may not rely upon the arrangement shown in Fig. 10 since it is in error and

instead represents something other than stacked diodes. In view of this, Applicants submit that the Jun et al. reference does not show the elements of claim 1 and especially does not show stacked diodes between a first power line and the I/O pad, as is required in claim 1.

Rejection of claims 13-17 as being anticipated by Jun et al.

Claim 13 depends from claim 1 and further recites that the diode includes a PN junction diode formed by a PN junction between a first source/drain and a substrate of a MOS. The Examiner states that this junction occurs between a first source/drain 14 and the substrate. However, Applicants submit that element 14 is not a source or drain of the MOS. Instead the source/drain regions are described as an element 32 in column 3, line 28. Thus, Applicants submit that the Examiner has misapplied the reference in regard to this feature and that claim 13 is further allowable. Claims 14-17 depend from claim 13 and are likewise additionally allowable.

Rejection of claims 2-4 as being obvious over Jun et al.

In regard to claim 2, the Examiner identifies the first well as region 16 and the deep well as region 12. the Examiner admits that the reference does not show a doped area in the first well but that this would have been obvious. Applicants submit that it would not be obvious to insert such a region since there is no indication of doing so and no motivation for providing such a region. Accordingly, Applicants submit that claim 2 is further allowable. Claim 4 depends from claim 2 and as such is also considered allowable.

Claim 3 also depends from claim 2 and is allowable as well. In addition, Applicants submit that region 16 is not a well as suggested by the Examiner and that the Examiner's

reading that region 16 is surrounded by well 12 is not appropriate. Accordingly, Applicants submit that claim 3 is further allowable.

Rejection of claims 5-12 as being obvious over Jun in view of Watt

In regard to claim 5, the Examiner points out that the Watt reference shows an ESD clamp circuit 24 and that it would have been obvious to use such a circuit in the device of Jun et al. However, Applicants wish to point out that claim 5 also states that the clamp circuit is set between a first power line and a second power line. In Watt, there are two clamps 24 and 26 and these do not extend between the power supply buses. Accordingly, Applicants submit that claim 5 is additionally allowable since the Watt reference does not show the feature as presently claimed.

Claim 11 depends from claim 5 and accordingly is also allowable. Claim 12 depends from claim 1 and further describes that one of the diodes is an MOS diode with a gate coupled to a source/drain. The Examiner states that Watt shows an MOS diode and it would have been obvious to one skilled in the art to provide secondary ESD protection. However, the Examiner has not indicated why such a diode has such a gate coupled to a source/drain of the diode. Accordingly, Applicants submit that claim 12 is further allowable.

The Examiner also rejected claim 15 over the combination of Jun et al. and Watt. Applicants submit that this claim is allowable based on its dependency from claim 13 as indicated above. Further, Applicants submit that the Examiner has not shown the connection of the gate to a second source/drain as recited in claim 15. Accordingly, Applicants submit that this claim is additionally allowable.

Claim 6-8 depend from claim 5 and as such are also considered to be allowable. In addition, claim 6 states that the two source/drains are coupled through the first and second

power lines. In the reference, the source and drain are not connected to V_{SSI} and V_{DDI} . Instead they are connected to V_{SSI} and V_{SSO} . Accordingly, Applicants submit that claim 6 is further allowable. Claim 7 and 8 depend from claim 6 and as such are also considered to be allowable. Further, claim 7 describes a gate applied with a bias voltage. Applicants submit that this is not seen. Likewise, claim 8 describes a gate applied with a bias voltage. Accordingly, Applicants submit that claims 7 and 8 are further allowable.

Claims 9 and 10 depend from claim 5 and as such are also considered to be allowable. In addition, claim 9 describes the arrangement of the wells. The Examiner agrees that the Watt reference does not show this arrangement but feels it would have been obvious to provide device isolation. Applicants submit that this would not be obvious since there are no teachings in the reference of the need to do so and no indication that such isolation is necessary. Accordingly, Applicants submit that claims 9 and 10 are additionally allowable.

IX. CONCLUSION

In summary, the various rejections given by the Examiner are in error. It is believed that Appellants have encountered all of the reasons given for the rejections of the appealed claims and thus these rejections do not appear to be proper. Accordingly, it is respectfully requested that this board reverse the rejections of claims 1-17.

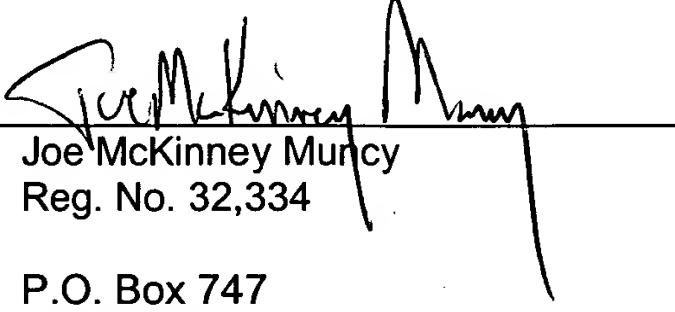

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Appellants respectfully petition for a one (1) month extension of time for filing the Appeal Brief. The required fee of \$110.00 was paid to the U.S. Patent and Trademark Office at the time of filing the original Appeal Brief on March 1, 2004.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
BIRCH STEWART KOLASCH & BIRCH LLP

Date: January 4, 2006

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0941-0316P

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APPENDIX OF CLAIMS



X. Claims appealed

1. An electrostatic discharge (ESD) protection circuit with low input capacitance, suitable for an I/O pad, comprising a plurality of diodes, stacked and coupled between a first power line and the I/O pad, wherein during normal operation, the diodes are reverse-biased, and, when an ESD event occurs between a second power line and the I/O pad, the diodes are forward-biased to conduct ESD current.

2. The ESD protection circuit as claimed in claim 1, wherein each diode is a PN junction diode formed by placing a doped area of a first conductivity type in a first well of a second conductivity type, a deep well of the first conductivity type formed under the first well to isolate the first well from a substrate of the second conductivity type.

3. The ESD protection circuit as claimed in claim 2, wherein the first well is surrounded by a second well of the first conductivity type.

4. The ESD protection circuit as claimed in claim 2, wherein the first conductivity type is N type, and the second conductivity type is P type.

5. The ESD protection circuit as claimed in claim 1, wherein the ESD protection circuit further includes a power-rail ESD clamp circuit, set between a first power line and a second power line, the power-rail ESD clamp circuit being turned on to conduct ESD current when an ESD event occurs.

6. The ESD protection circuit as claimed in claim 5, wherein the power-rail ESD clamp circuit includes a substrate-triggered MOS of the first conductivity type, the substrate-

triggered MOS including two source/drains and a substrate, the two source/drains coupled to the first power line and the second power line respectively, the substrate node biased with suitable current to trigger a bipolar junction transistor parasitizing in the substrate-triggered MOS, and conducting ESD current when an ESD event occurs.

7. The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS includes a gate applied with a bias voltage to keep the substrate-triggered MOS off during normal operations.

8. The EDS protection circuit as claimed in claim 6, wherein the gate is applied with a bias voltage to speed up the turn-on rate of the substrate-triggered MOS when an ESD event occurs.

9. The ESD protection circuit as claimed in claim 6, wherein the substrate-triggered MOS is formed in a first well of a second conductivity type, a deep well of a first conductivity type being formed under the first well to isolate the first well from a substrate of the second conductivity type.

10. The ESD protection circuit as claimed in claim 9, wherein the first well is surrounded by a second well of the first conductivity type.

11. The ESD protection circuit as claimed in claim 5, wherein the power-rail ESD clamp circuit includes an ESD detection circuit to detect the occurrence of the ESD event.

12. The ESD protection circuit as claimed in claim 1, wherein one of the diodes is a MOS diode with a gate coupled to a source/drain of the MOS diode.

13. The ESD protection circuit as claimed in claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain and a substrate of a MOS.

14. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to the first power line.

15. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to a second source/drain of the MOS.

16. The ESD protection circuit as claimed in claim 13, wherein the MOS is PMOS.

17. The ESD protection circuit as claimed in claim 13, wherein the MOS is NMOS.

Evidence Appendix

None

Related Appeals and Interferences Appendix

None